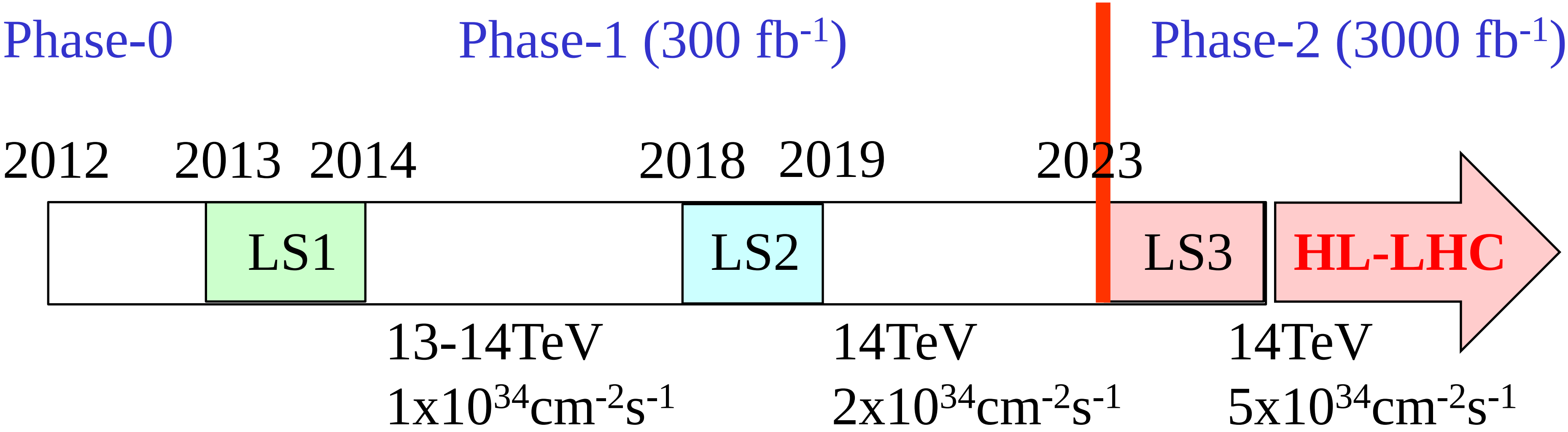
Novel Techniques and Detectors for Pile-up Mitigation for HL-LHC

’14 8/25 Y.Takubo (KEK)

On behalf of ATLAS & CMS collaboration

LHC upgrade plan toward HL-LHC



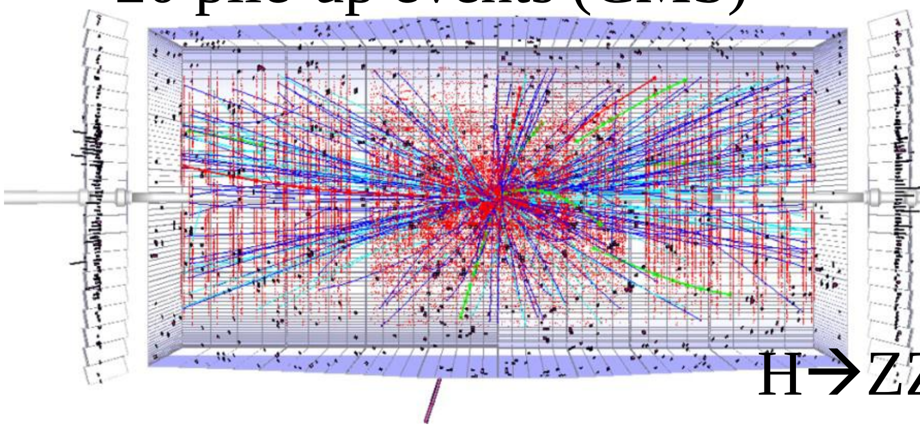
- HL-LHC is planed to start around 2024.
- Nominal instantaneous luminosity: 5×10^{34} cm^{-2}s^{-1}
  - ➢ The maximum peak luminosity: 7×10^{34} cm^{-2}s^{-1}
- The instantaneous luminosity becomes 2.5~3.5 times larger, compared to the end of phase-1.
- Deliver the integrated luminosity of 3000 fb^{-1}

Pile-up condition in HL-LHC

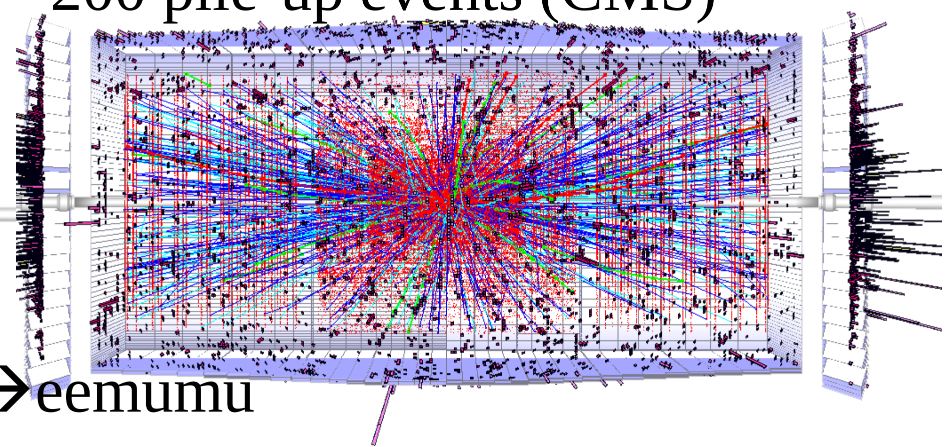
- The number of interaction is 140 per bunch crossing at 5×10^{34} cm^{-2}s^{-1}.
  - 55 pile-up events at 2×10^{34} cm^{-2}s^{-1}
- 200 pile-up events at the maximum peak luminosity of 7×10^{34} cm^{-2}s^{-1}
- The pile-up gets 2.5~3.5 times larger than phase-1.
- The pile-up mitigation is important to keep the detector performance.

The technique for the pile-up mitigation for HL-LHC (+ upgrade during LS2) will be presented based on the upgrade of ATLAS and CMS.

20 pile-up events (CMS)



200 pile-up events (CMS)

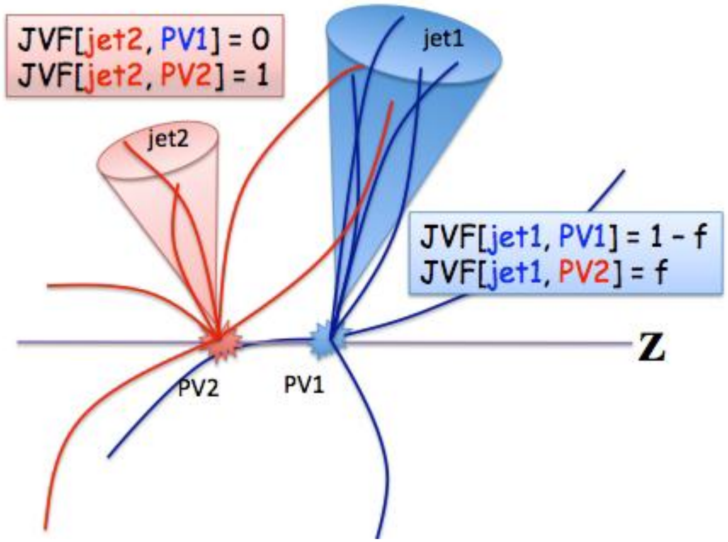


H→ZZ→eemumu

Pile-up effects

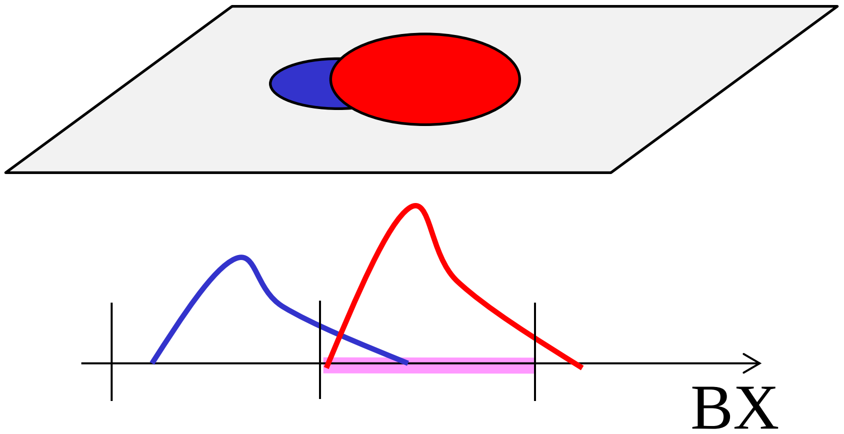
In-time pile-up

- The pile-up happens from several pp interactions per bunch crossing due to high luminosity.
- Mis-association of the tracks from other collisions makes worse for the jet energy measurement.



Out-of-time pile-up

- Effects from particles of the previous bunch crossings due to slow or uncorrected detector response.

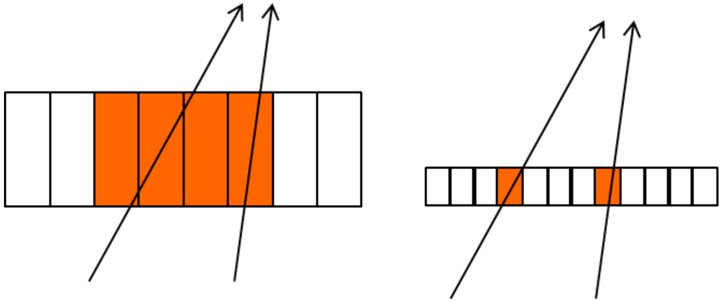


Basic idea for pile-up mitigation (1)

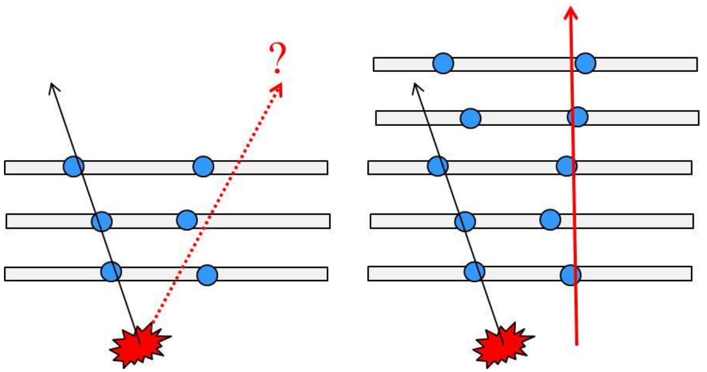
Several possible solution is under consideration for the pile-up mitigation in ATLAS and CMS for LH-LHC.

Tracking

- High granularity and thin active region



- Increase the number of the tracking layers

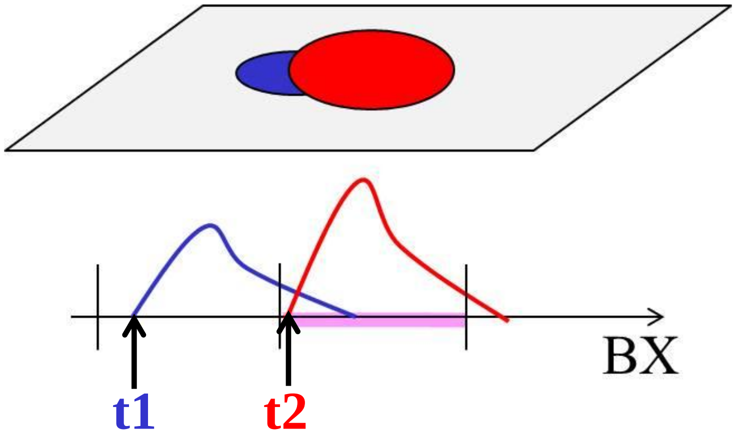


- Remove hits coming from low-pT particles

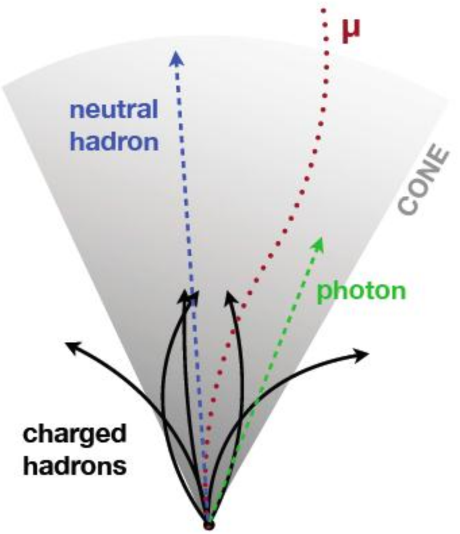
Basic idea for pile-up mitigation (2)

Calorimetry

- Application of the hit timing information.



- Energy measurement of individual particles with particle flow technique.
  - Charged particle: Tracker
  - Photon: ECAL
  - Neutral hadron: HCAL
  - This technique is already used in CMS, so that skipped in this talk.



Let's check the effort to realize these solutions in ATLAS and CMS!

Silicon sensor with high granularity and thin active region

High granularity and thin pixel detector

	Current ATLAS		ATLAS at HL-LHC
Inner layers			
• Pixel size (um^2):	50 x 250	x 0.3	25 x 150
• Thickness (um):	200	x 0.75	150
Outer layers			
• Pixel size (um^2):	50 x 400	x 0.63	50 x 250
• Thickness (um):	250	x 0.6	150

	Current CMS		CMS at HL-LHC
• Pixel size (um^2):	100 x 150	x ~0.3	<50 x 100
• Thickness (um):	285		100~300

The pixel hit occupancy can be kept at the same level as phase-1 with 3.5 times larger pile-up in HL-LHC.

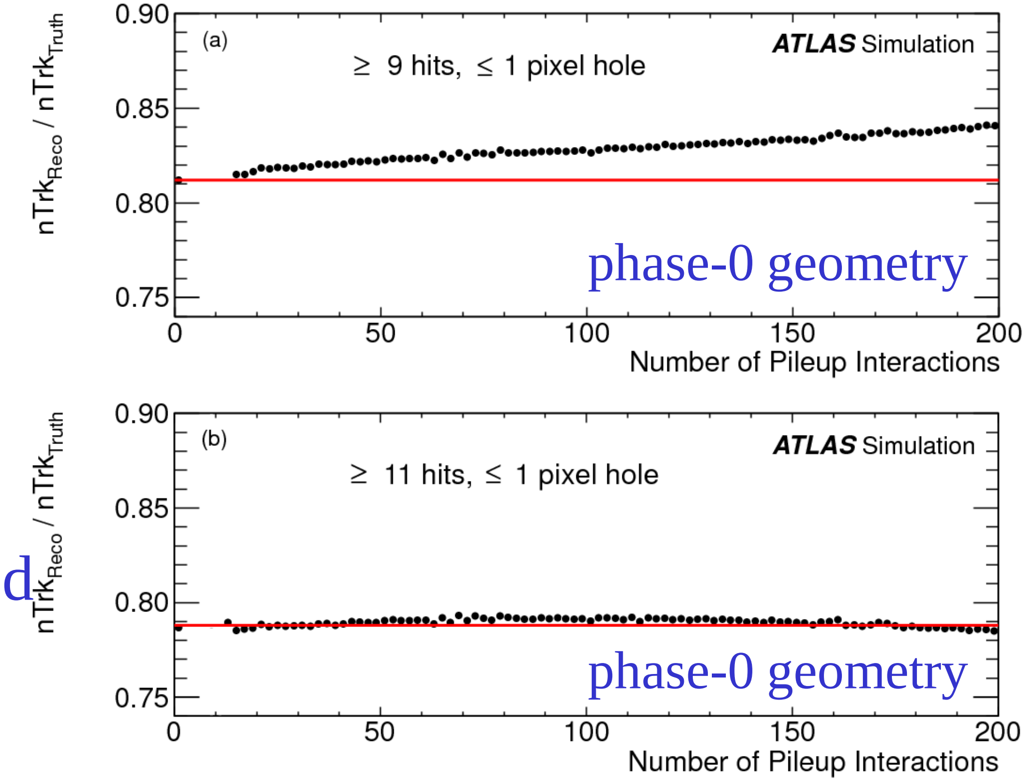
Increasing # of tracking layers

Hit points and tracking

- The tracking performance cannot be maintained with current silicon trackers in ATLAS and CMS.
- Increasing the number of hit points in the silicon trackers significantly improves the tracking performance in high pile-up condition.

Ratio of # of rec. and true track (tt events)

- For example, ATLAS can keep the performance with 11 hits with phase-0 geometry.
  - With 3 pixel layers



The silicon layers will be increased in HL-LHC.

ATLAS silicon layer

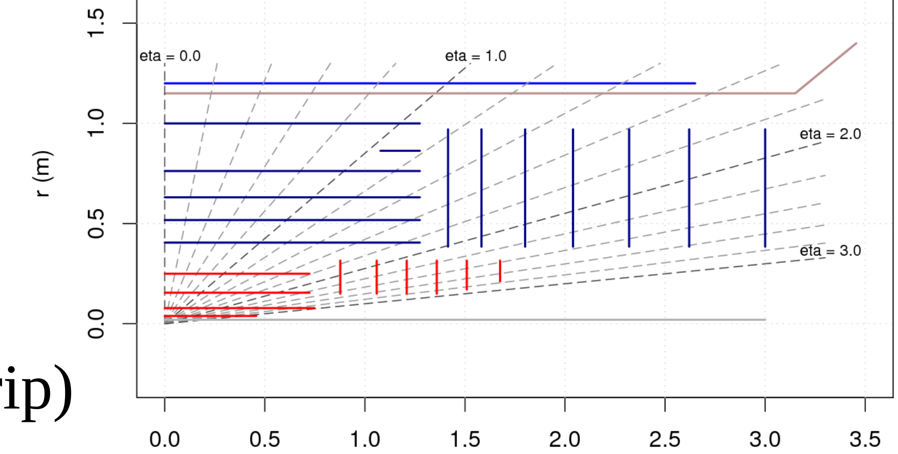
Current ATLAS silicon layout

- Barrel: 4 pixel/4 strip
- End-cap: 3 pixel/9 strip

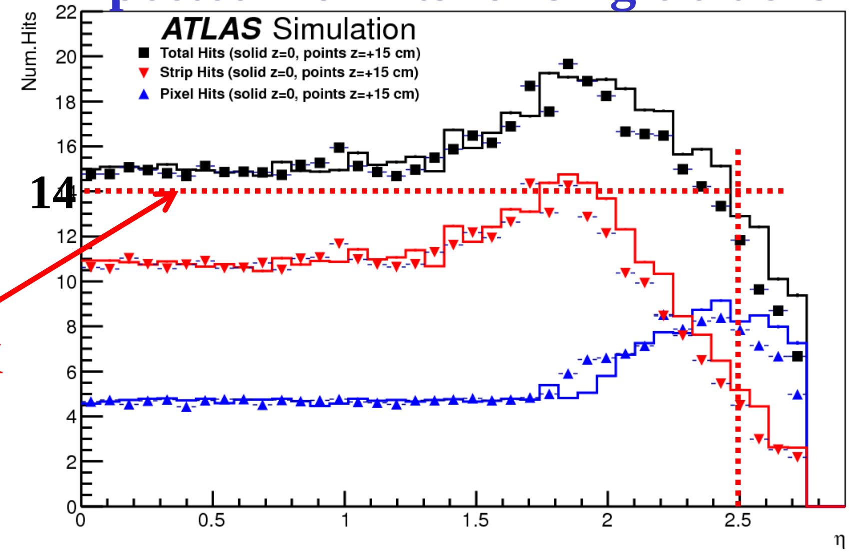
New silicon layout for LH-LHC

- Barrel: 4 pixel/5 strip (or 5 pixel/5 strip)
- End-cap: 6 pixel /7 strip
- For ATLAS, the silicon layer will be increased also to compensate for removing TRT.
- Aim at least 14 hits for one single track

ATLAS baseline layout of Si-tracker for LH-LHC



Expected # of hits for single tracks



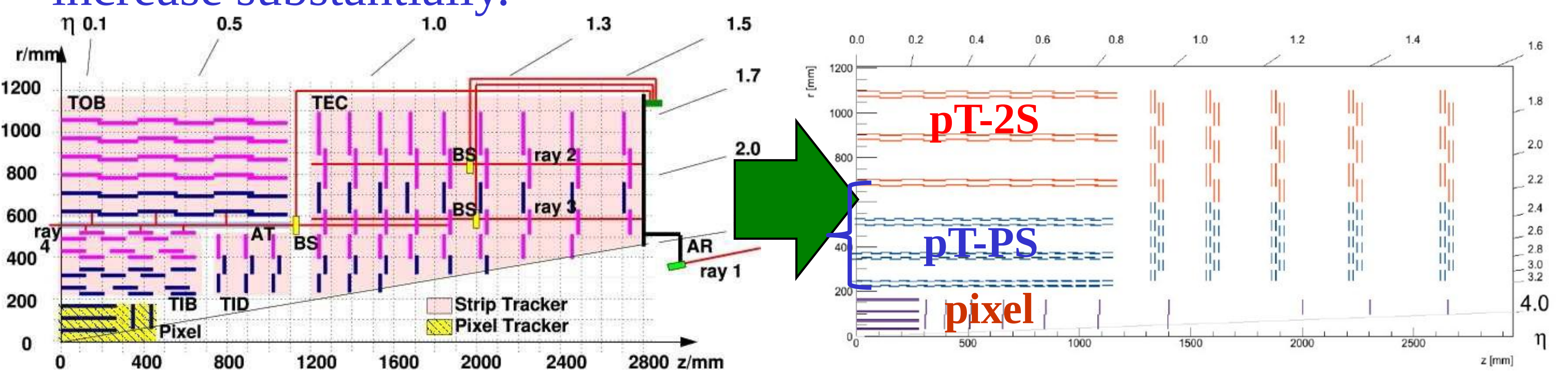
CMS silicon layer

Current CMS silicon layout

- Barrel: 3 pixel/10 strip (→ The 4th pixel layer will be added in LS2.)
- End-cap: 2 pixel/12 strip

New silicon layout for LH-LHC

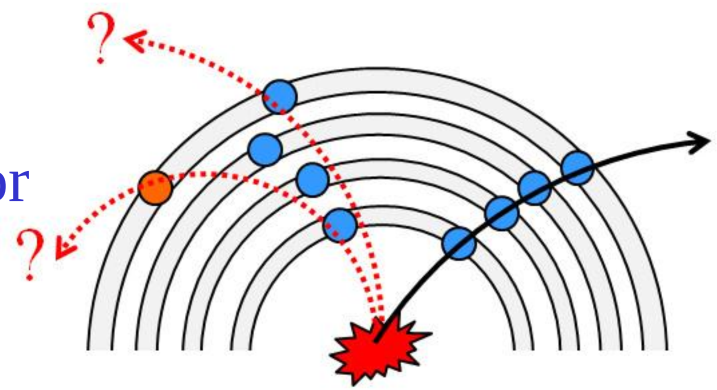
- Barrel: 4 pixel/3 pT-PS modules/3 pT-2S modules
- End-cap: 10 pixel /5 pT-PS module/5 pT-2S module
- Since each pT-module has two sensor, the silicon layers will much increase substantially.



Rejection of low pT hits

Rejection of low pT track (1)

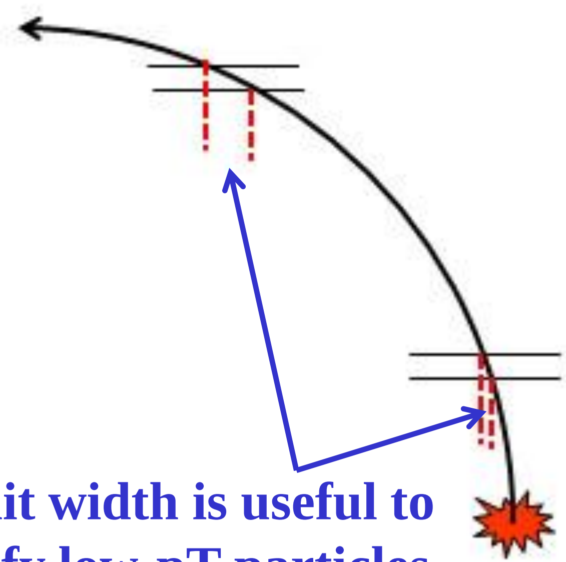
- The hits with low-pT particles degrade the performance of the track reconstruction.
- If low-pT hits can be rejected in the detector level, it will help pile-up mitigation.



- Low-pT tracks have larger curvature in the magnetic field.

→ Can we identify the low-pT hits by using the hit width in the detector?

- The strong B-field of CMS (4T) can realize this method.



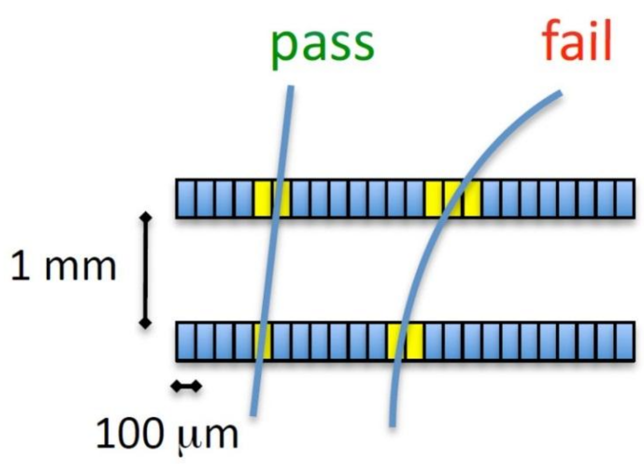
The hit width is useful to identify low-pT particles

pT-modules have been developed in CMS.

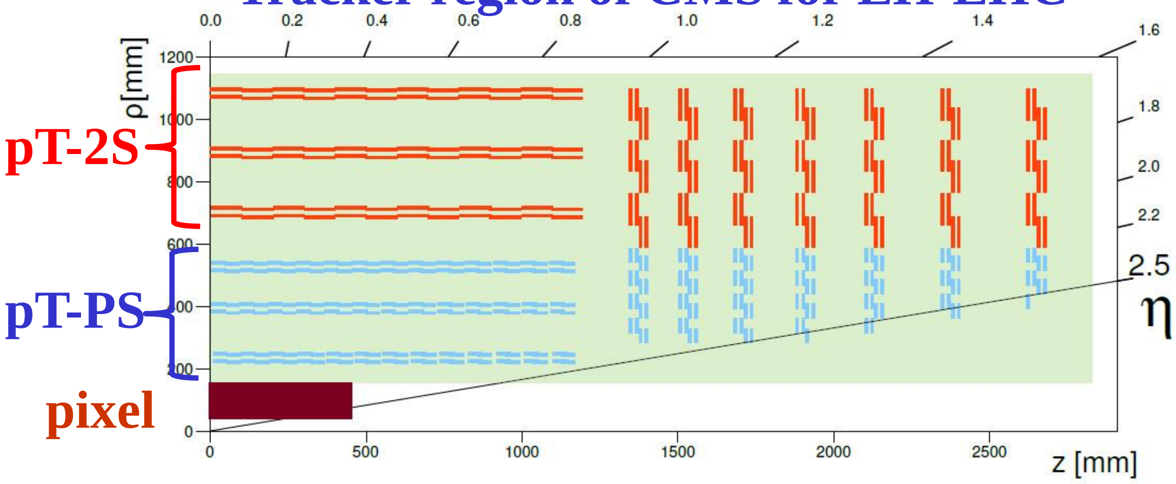
Rejection of low pT track (2)

pT module

- Consists of two closely spaced silicon sensors
  - Two sensor gap: 2~4 mm
- The correlated hits on the two sensors will be used to find low pT tracks (<2GeV).
- pT-module will be used as the tracker instead of the usual strip detector.
- pT-PS and pT-2S modules have been developed.



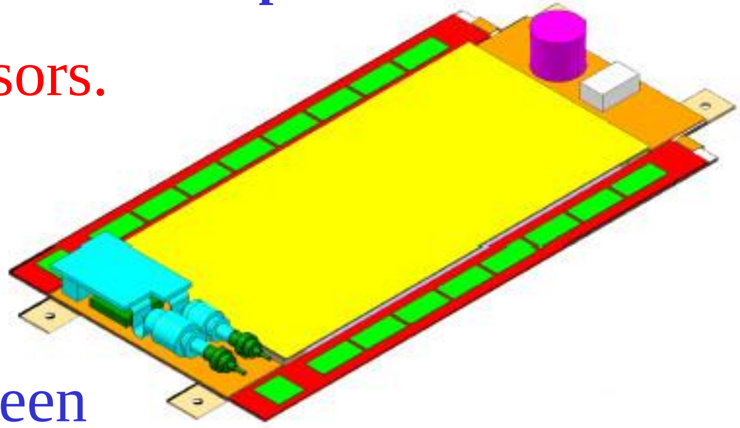
Tracker region of CMS for LH-LHC



Rejection of low pT track (3)

pT-PS module

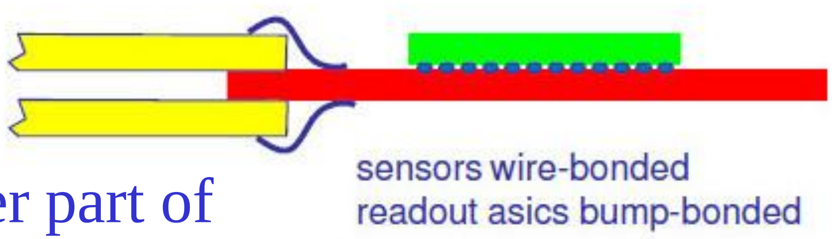
pT-PS module



- The combination of the pixel and strip sensors.
- Pixel size: 1.5mm x 100um
- Strip size: 2.5cm x 100um
- They will be put at the middle region between pixel and outer region (20cm < R < 60cm)

pT-2S module

pT-2S module



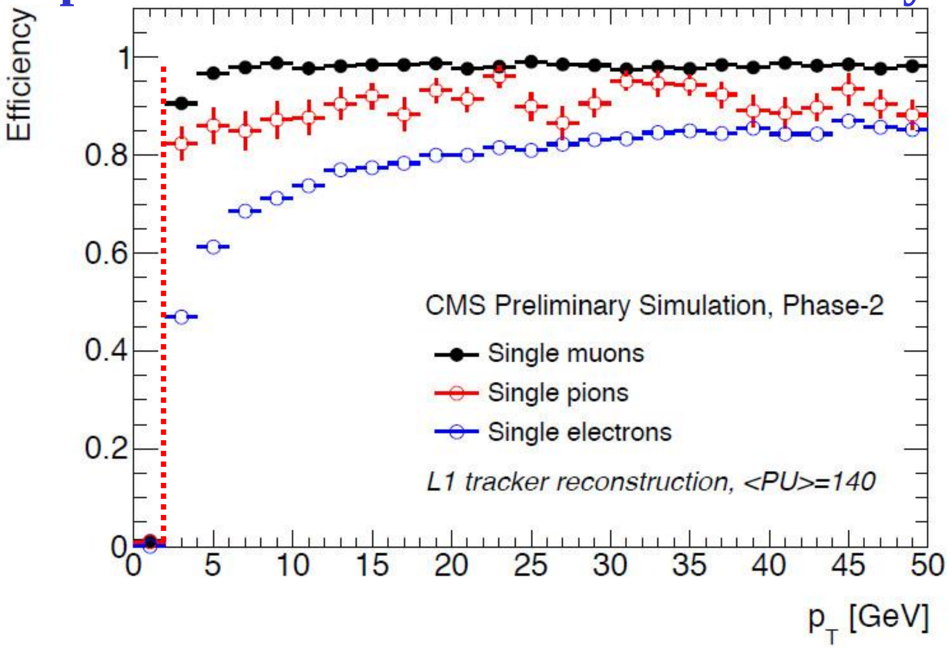
- Sandwich structure of 2 strip sensors.
- Strip size: 5cm x 90um
- The modules will be placed at the outer part of the tracker (60cm < R <120cm)

Rejection of low pT track (4)

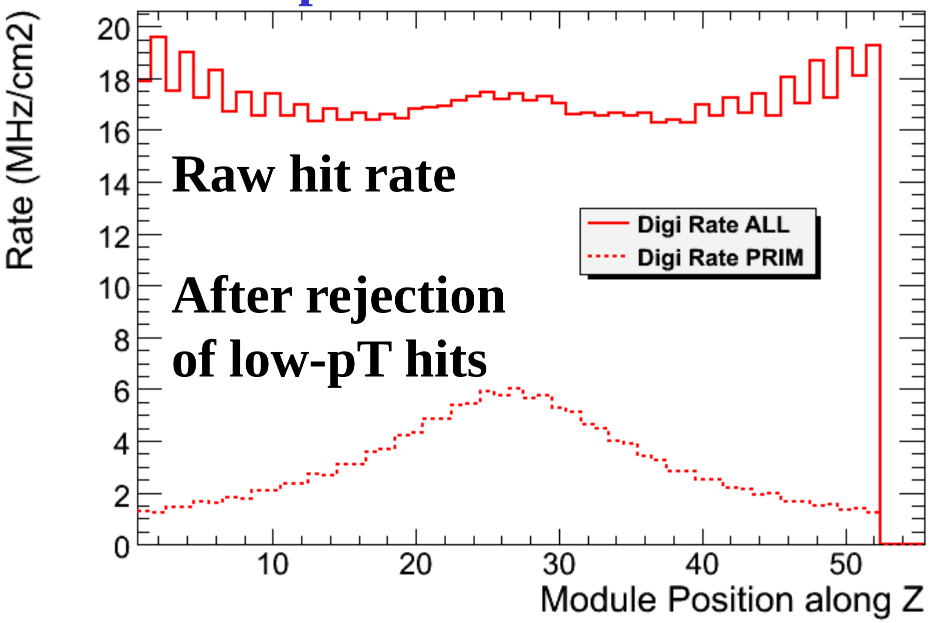
- The tracker with pT-modules can efficiently reject the particles below 2 GeV/c.
- pT-module also help to reduce the data size by 10~30%, comparing to the situation without any hit rejection.

→ pT-module is very powerful tool for the pile-up mitigation.

pT v.s. Track reconstruction efficiency



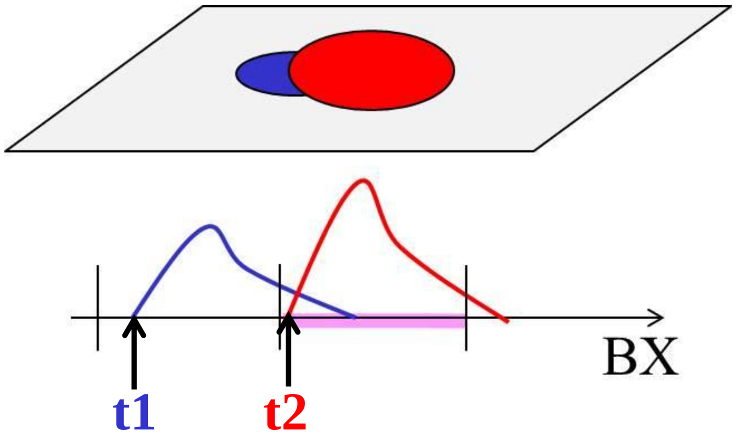
Z position v.s. Hit rate



Reducing out-of-time pile-up

Reducing out-of-time pile-up (1)

- Out-of-time pile-up degrades the energy resolution of the calorimeter.
- This happens due to slow integration time in readout electronics.
  - CMS HCAL: ~50 ns
- If the hit timing is usable, out-of-time pile-up can be rejected efficiently.

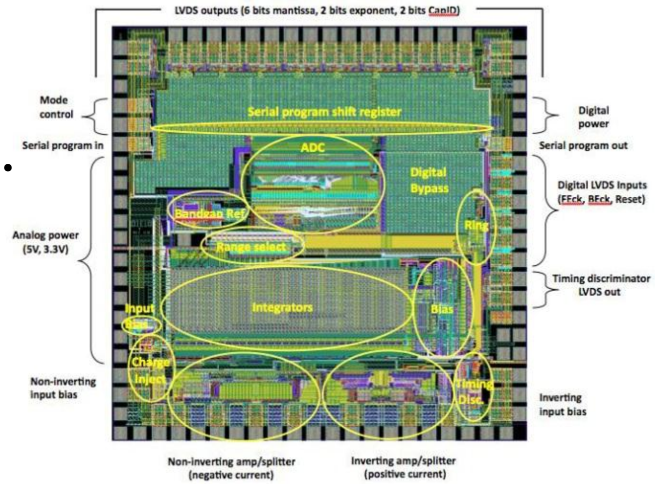


The readout system will be upgraded for CMS HCAL during LS2 to use the timing information.

Reducing out-of-time pile-up (2)

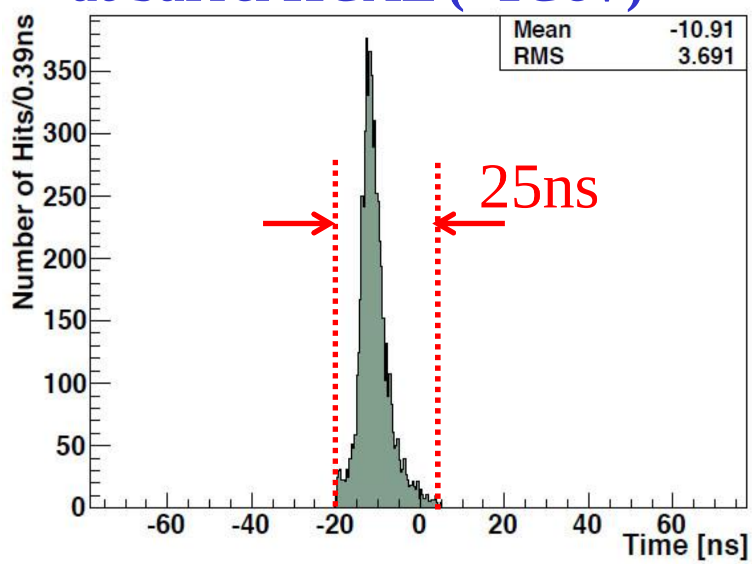
Challenge in CMS HCAL

- The current ASIC gives only ADC information.
- New readout ASIC will be developed for HCAL in the upgrade during LS2 to give the timing information.
  - TDC timing resolution: 0.5 ns



- Hits of particles with energy above 1GeV can be identified within the bunch crossing time.

Simulated TDC distribution at barrel HCAL (>1GeV)

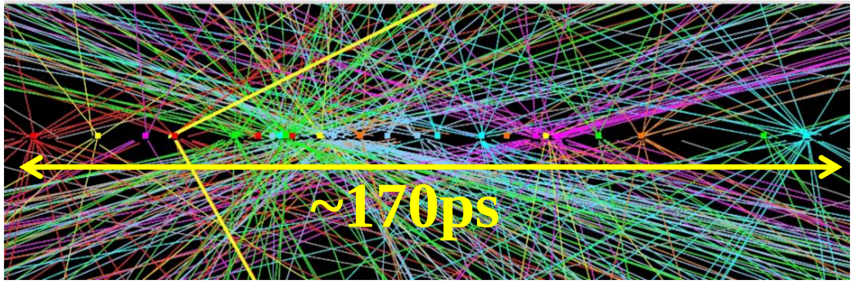


The out-of-time pile-up will be solved.

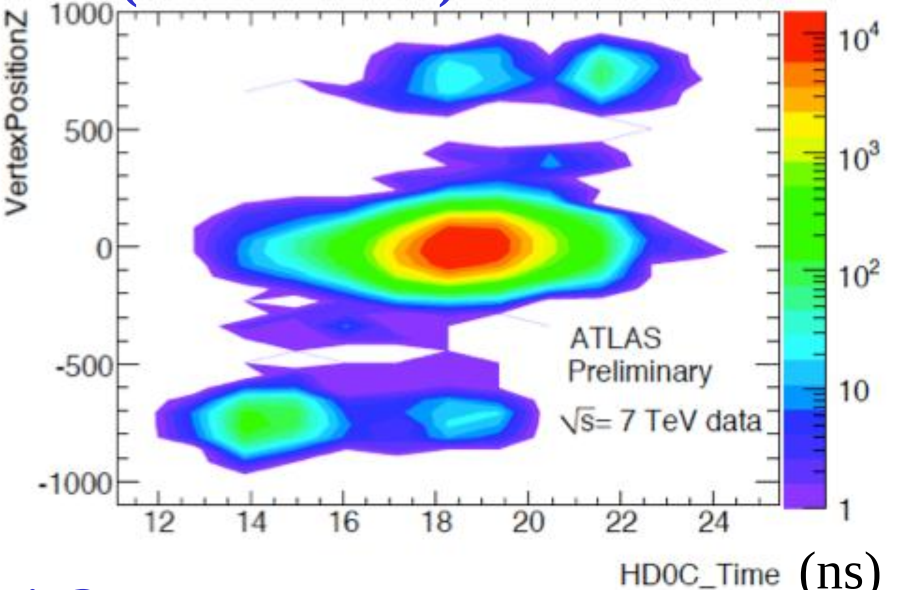
Aggressive idea to use timing

Aggressive method to use timing (1)

- If the timing of each collision in the same beam crossing can be identified, in-time pile-up can be rejected.
- Time resolution of ~20 ps is needed.
  - The interaction time of a bunch crossing: ~170 ps (rms)
- ATLAS and CMS have calorimeters with good timing resolution.
  - ATLAS ZDC: 200 ps
  - Still not enough for identification of the collision timing.

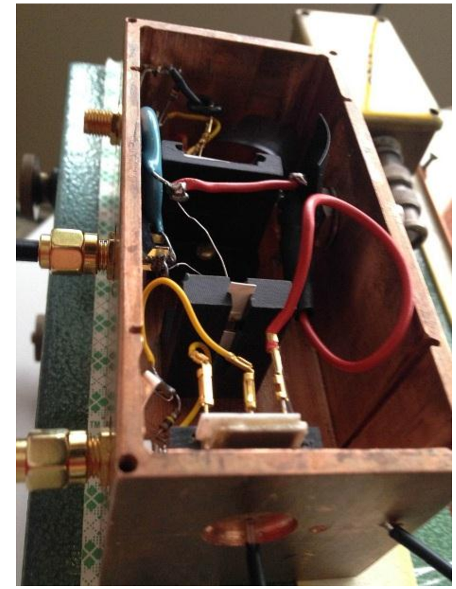


Timing v.s. vertex position (ATLAS ZDC)



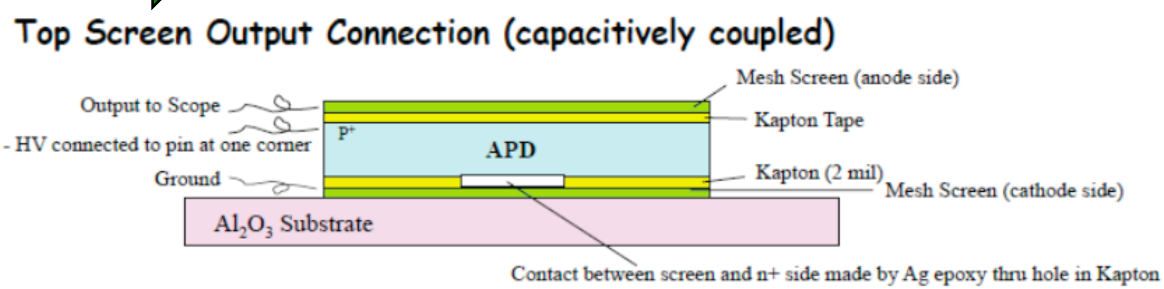
Is the time resolution of ~20 ps realistic?

Aggressive method to use timing (2)



- Implementation of the dedicated timing plane is under consideration in CMS endcap region for LH-LHC. (still it is not decided yet to put it.)
- There are several detector candidates:
  - Special capacitive readout APD with Micro Megas field shaping
  - MicroMegas photo-detector with MgF_2 window to make Cherenkov UV photons
- APD-option achieved 20 ps res. in testbeam.

In-time pile-up might be resolved!



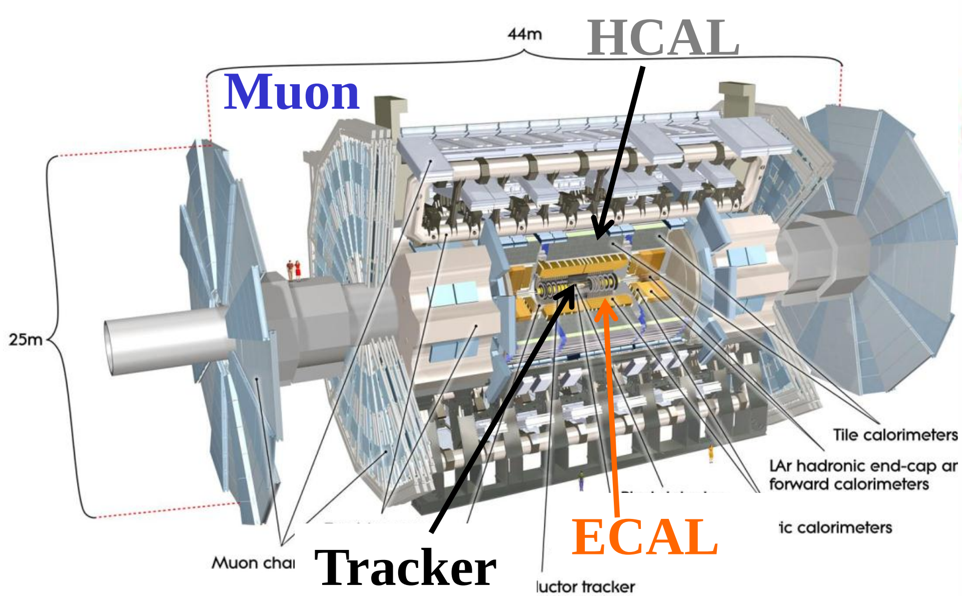
See arXiv:1309.7985 [physics.ins-det]

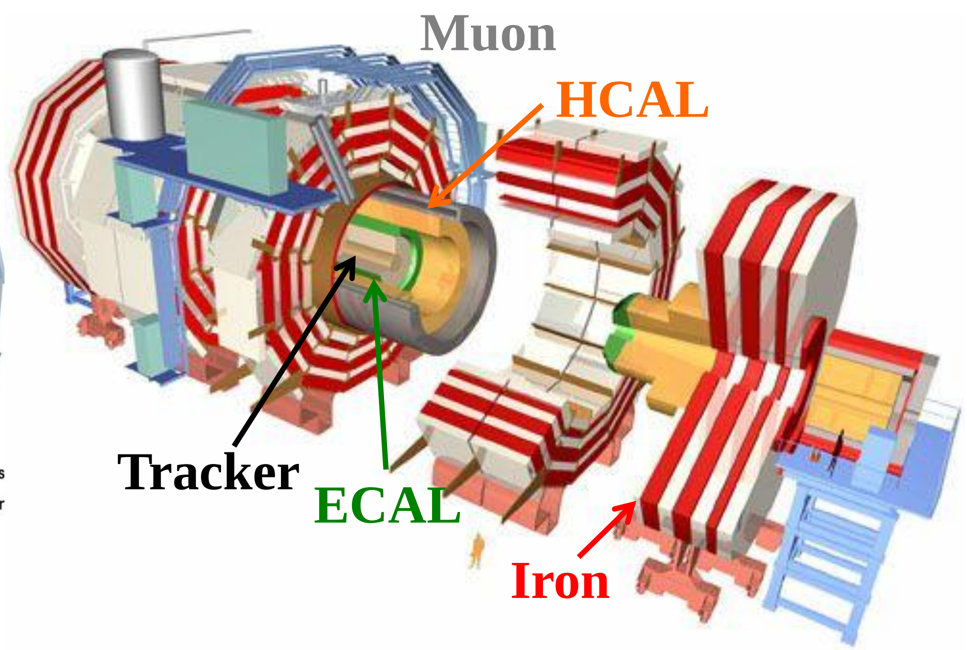
Summary

- The pile-up mitigation is very important topic for the detector at HL-LHC to maintain their detector performance.
- ATLAS and CMS will be upgraded to mitigate high pile-up condition.
  - Higher granularity and thinner silicon sensor.
  - Larger number of the silicon layers.
  - Rejection of low-pT hits by using the hit pattern in the silicon tracker.
  - Precise timing information to reject out-of-time pile-up.
- Upgraded ATLAS and CMS will show better performance of the pile-up mitigation even at the condition of HL-LHC.

Current ATLAS & CMS detectors

	ATLAS	CMS
Inner tracker	Si tracker (pixel+strip), TRT	Si tracker (pixel + strip)
ECAL	Liquid Ar	$PbWO_4$
HCAL	Sci. tile + absorber(steel)	Sci tile + absorber (brass or steel)
B-field	2T solenoid + 0.5&1T toroidal	3.8T solenoid
Mon detector	MDT, TGC, RPC, CSC	DT, CSC, RPC





High granularity strip detector (1)

	Current ATLAS		ATLAS at HL-LHC
<u>Inner barrel layers</u>			
• Strip pitch (um):	80		74.5
• Strip length (cm)	12.8	x ~ 0.2	2.4
• Thickness (um):	300		320 (might be 250)
<u>Outer barrel layers</u>			
• Strip pitch (um):			74.5
• Strip length (cm)			4.8
• Thickness (um):			320

The strip hit occupancy can be less than phase-1 with 3.5 times larger pile-up in HL-LHC.

High granularity strip detector (2)

Inner barrel layers	Current CMS		CMS at HL-LHC	
• Strip pitch (um):	80, 120	x 0.24	100	Pixel size of pT-PS module
• Strip length (cm)	6.33		1.5	
• Thickness (um):	320		<=320	

Outer barrel layers				
• Strip pitch (um):	122, 183	x 0.74, 0.49	90	Strip size of pT-2S module
• Strip length (cm)	9.64	x 0.52	5	
• Thickness (um):	500		<=500	

- The module with two closely spaced sensors (pT-module → see later slides) will be used instead of the current strip detector.
  - pT-PS: pixel + strip sensors, pT-2S: 2 strip sensors
- The tracker occupancy will get much lower than phase-1 with 3.5 times larger pile-up in HL-LHC.